

REMARKS:

The Office Action dated September 12, 2000, has been received and carefully noted. The above amendments and the following remarks are submitted as a full and complete response thereto.

As a preliminary matter, Applicant respectfully submits that some of the information on Form PTO-892 which accompanied the Office Action, is incorrect. More specifically, the patent number cited for Fernandez et al. was "5,448,209," and should be --5,448,200--. In addition, the "Date" referred to for Harris et al. was "9/1998." The correct date is -- December 12, 1995 or 12/1995--. Applicant has attached a marked-up Form PTO-892 indicating the corrections therein. Therefore, Applicant respectfully requests issuance of a new Form PTO-892 with the correct information therein.

Applicant thanks the Examiner for indicating allowable subject matter in claim 6-15 and 20. Claims 1 and 6 have been amended to more particularly point out and distinctly claim the subject matter of the invention. No new matter has been added by the above noted amendments. Therefore, claims 1-20 are respectfully submitted for consideration.

Claims 1-15 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Applicant respectfully submits that the above amendments to claims 1 and 6 should be sufficient to overcome the deficiencies noted in the Office Action and place these claims in compliance with US patent practice. Accordingly, Applicant respectfully submits that claims 6-15 are now in condition for allowance.

Claims 1-5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Harris et al. (U.S. Patent No. 5,475,323, hereinafter "Harris"). The Office Action took the position that Harris disclosed all of the elements of the claimed invention with the exception

of showing, the input terminals are connected to a reference voltage and an external signal, respectively. The Office Action stated that it would have been obvious to a person of ordinary skill in the art "to apply an external signal and a fixed reference input voltage to the input terminals of Harris for purpose of operating the circuit as a threshold comparator." Applicant respectfully traverses this rejection, and submits that each of Claims 1-5 recites subject matter which is neither disclosed nor suggested in the cited prior art.

Claim 1, upon which claims 2-5 are dependent, recites an input circuit comprising a differential circuit including a first transistor for receiving an external signal and a second transistor for receiving a reference signal, wherein sources of the first and second transistors are connected in common, and the differential circuit generates an internal signal in accordance with a current flowing through the first and second transistors. In addition, the input circuit comprises a current regulating circuit connected to the differential circuit, wherein the current regulating circuit regulates an amount of the current flowing through the differential circuit in response to the internal signal.

Accordingly, the present invention provides input circuits which amplify external signals to generate internal signals having predetermined amplitudes. In order to achieve this advantage, semiconductor memory devices are provided with input circuits which amplify external input signals to generate internal input signals having predetermined amplitudes. An input circuit generates internal input signals which rise and fall in response to the rising edges and falling edges of external input signals.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the presently pending claims and, therefore, fails to provide the critical and nonobvious advantages which are provided by the present invention.

Harris discloses an integrated circuit apparatus and method provided for utilizing voltage dividers and differential amplifiers. Harris discloses three integrated circuit resistors R_1 , R_2 , and R_3 . The resistors have a length L_1 , L_2 and L_3 , and width W_1 , W_2 and W_3 , respectively. The voltage drop between node 101 and node 100 is V_{in} , the voltage drop between node 102 and node 100 is V_{out1} , and the voltage drop between node 103 and node 100 is V_{out2} . Harris also discloses a microelectronic resistor voltage divider 20 with linearly spaced output taps. In order to contact voltage divider 20, accessible outputs or tap connections are provided. Adding taps to voltage divider 20 will result in the creation of parasitic tap resistances between tap connection sites 28 and 30 and main body 34 of voltage divider 20. The effect of a tap is to place parasitic resistors, r_t , associated with the tap in parallel with small resistor segments, r_a , of the body of the resistor that is effected by r_t .

Applicant respectfully submits that claim 1 provides for the features, among others, of "...the differential circuit generates an internal signal..." and "a current regulating circuit connected to the differential circuit, wherein the current regulating circuit regulates the amount of current flowing through the differential circuit in response to the internal signal." (Emphasis added). Applicant respectfully submits that the aforementioned features are not disclosed, taught or suggested by Harris. In particular, Figure 25 of Harris fails to disclose or suggest an internal signal , wherein the current regulating circuit regulates the amount of current flowing through the differential circuit in response to the internal signal. Accordingly, applicant submits that claim 1 recites subject matter that is neither disclosed nor suggested by Harris. Furthermore, applicant submits that the subject matter is more than sufficient to render the claimed invention non-obvious to a person of ordinary skill in

the art. Therefore, applicant respectfully requests reconsideration of the rejection of claim 1 under 35 U.S.C. § 103(a).

With regard to claims 2-5, applicant submits that each of claims 2-5 recites subject matter which is neither disclosed nor suggested by nor is obvious over Harris. In particular, each of claims 2-5 depends on claim 1, and therefore, inherently incorporates each and every limitation recited within claim 1, therein. Therefore, in view of applicant's remarks noted above regarding claim 1, applicant submits that each of claims 2-5 also recites subject matter which is neither disclosed nor suggested by Harris, and that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art. Therefore, in view of the aforementioned remarks, applicant respectfully requests reconsideration of claims 1-5.

Claims 16-19 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over Fernandez et al. (U.S. Patent No. 5,448,200, hereinafter "Fernandez"). In making this rejection, the Office Action took the position that Fernandez disclosed all of the elements of the claimed invention with the exception of showing an input terminal receiving an external signal. The Office Action asserted that it would have been obvious to one of ordinary skill in the art "to supply an external signal to an input terminal of Fernandez for the purpose of providing a threshold comparator." Applicant respectfully traverses this rejection, and submits that each of Claims 16-19 recites subject matter which is neither disclosed nor suggested in the cited prior art.

Claim 16, upon which claims 17-20 are dependent, recites an input circuit comprising a first MOS transistor, a second MOS transistor, a third MOS transistor, a fourth MOS transistor, a fifth MOS transistor, a six MOS transistor and a first inverter. The first

MOS transistor has a gate that receives a data signal. The second MOS transistor has a gate connected to a reference voltage, wherein the source of the first transistor is connected to the source of the second transistor at a first node. The third MOS transistor is connected between the first node and a low potential power supply, and having its gate connected to a high potential power supply. The fourth MOS transistor connected is connected between the first node and the low potential power supply. The fifth MOS transistor is connected between the drain of the first transistor and the high potential power supply. The sixth MOS transistor is connected between the drain of the second transistor and the high potential power supply, wherein the gates of the fifth and sixth transistors are connected to each other and to the drain of the sixth transistor. The first inverter has an input terminal connected to a second node between the first and fifth transistors and an output terminal connected to the gate of the fourth transistor.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the presently pending claims and, therefore, fails to provide the above critical and non-obvious advantages which are provided by the present invention.

Fernandez discloses a master-slave differential comparator having a threshold value. Fernandez discloses a differential comparator 1, with two inputs (IN+, IN-), as having a master section 3 and a slave section 2. The master section 3 (having an output TSET and having inputs) coupling to fixed biases), where A is the differential threshold value for the comparator. The slave section (responsive to the two comparator inputs IN+, IN- and to the output TSET of the master section) compares signals on the two comparator inputs and produces an output (OUT+, OUT-) when the signals differentially exceed the differential threshold value. A signal on OUT+ is asserted when a signal on IN+ exceeds a

signal IN- by delta and a signal on OUT- is asserted when the signal IN- exceeds the signal IN+ by delta.

Applicant respectfully submits that claim 16 recites many features including six MOS transistors, wherein the sixth MOS transistor is connected between the drain of the second transistor and the high potential power supply, wherein the gates of the fifth and sixth transistors are connected to each other and to the drain of the sixth transistor. Applicant respectfully submits that Fernandez does not disclose, teach or suggest the aforementioned features recited in the claimed invention. In particular, Figure 5 of Fernandez merely discloses five transistors connected in a manner wholly and completely different from the structure as claimed in the instant invention. Therefore, Applicant submits that claim 16 recites subject matter that is neither disclosed nor suggested by Fernandez, and applicant submits that the subject matter is more than sufficient to render the claimed invention non-obvious to a person of ordinary skill in the art.

With regard to claims 17-19, applicant submits that each of claims 17-19 recites subject matter which is neither disclosed nor suggested by Fernandez. In particular, each of claims 17-19 depends on claim 16, and therefore, inherently incorporates each and every limitation recited within claim 16, therein. Therefore, in view of applicant's remarks noted above regarding claim 16, applicant submits that each of claims 17-19 also recites subject matter which is neither disclosed nor suggested by Fernandez, and applicant submits that the subject matter is more than sufficient to render the claimed invention non-obvious to a person of ordinary skill in the art. Therefore, in view of the aforementioned remarks, applicant respectfully requests reconsideration of claims 16-19.

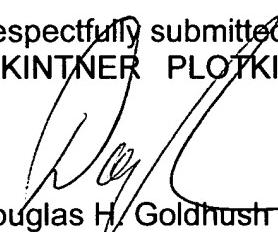
Given the above, applicant respectfully submits that claims 1-5 and 16-19 recite

subject matter which is neither disclosed nor suggested in the cited prior art. Applicants submit that this subject matter is more than sufficient to render the claimed invention nonobvious to a person of ordinary skill in the art. Applicant therefore respectfully submits that claims 1-20 are in condition for allowance and respectfully requests the application be passed to issue.

If for any reason the Examiner determines that the application is not in its present form in condition for allowance, it is respectfully submitted that the Examiner contact by phone the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees, may be charged to counsel's Deposit Account No. 01-2300.

Respectfully submitted,
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Enclosures: Notification of Change of Name and Address
 Form PTO-892 (w/corrections)